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VERIGY US, INC.

8  
9 UNITED STATES DISTRICT COURT  
10 NORTHERN DISTRICT OF CALIFORNIA  
11 SAN JOSE DIVISION

12 VERIGY US, INC, a Delaware Corporation

13 Plaintiff,

14 vs.

15 ROMI OMAR MAYDER, an individual;  
16 WESLEY MAYDER, an individual; SILICON  
TEST SYSTEMS, INC., a California Corporation;  
17 and SILICON TEST SOLUTIONS, LLC, a  
California Limited Liability Corporation,  
18 inclusive,

19 Defendants.

Case No. C07-04330 RMW (HRL)

**DECLARATION OF ROBERT  
POCHOWSKI IN SUPPORT OF  
PLAINTIFF'S REPLY AND  
SUPPLEMENTAL PAPERS RE:  
PRELIMINARY INJUNCTION**

Date: December 14, 2007

Time: 9:00 a.m.

Place: Courtroom 6

Judge: Hon. Ronald M. Whyte

Complaint Filed:

August 22, 2007

Trial Date:

None Set

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22  
23  
24 **CONFIDENTIAL**  
25 **DOCUMENT SUBMITTED UNDER SEAL**  
26  
27  
28

1 I, Robert Pochowski, declare as follows:

2 1. I am President of Attest Technologies. Prior to my current position, I worked at  
3 Agilent Technologies Inc. ("Agilent") from June 2004 to July 2005 as Vice President / General  
4 Manager of the California Semiconductor Test Division. After my departure, Agilent spun off a  
5 successor-in-interest, Verigy US, Inc. ("Verigy"). I have a B.S.E.E. from Marquette University  
6 and a MBA from Santa Clara University. I have been involved in semiconductor device testing  
7 for the last 27 years in various roles including engineering, R&D, marketing and management.  
8 Except for matters asserted on information and belief, which I am informed and believe to be true,  
9 I make this declaration of my personal knowledge and, if called as a witness, I could and would  
10 testify competently to the facts set forth herein.

11 2. When Mayder first approached me about the [REDACTED] I asked him if Verigy  
12 was doing anything similar or related to the proposed product. Mayder informed me that Verigy  
13 was not involved in anything similar, and it was on the basis of these representations that I agreed  
14 to work on the product with Mayder. In fact, he never told me that the Picasso ASIC was based  
15 on or related to work he had done at Verigy. If I had known that the Picasso ASIC was based on  
16 or related to work Mayder did at Verigy, I would not have agreed to work with him. The tester  
17 business is a relatively small world and I would not act in a way that would interfere with Agilent  
18 or Verigy or infringe upon their intellectual property rights, and I still maintain friendships with  
19 several Verigy employees.

20 3. One of the reasons I was interested in the Picasso ASIC was because I thought it  
21 was a unique product. I never told Mayder, as he states in paragraph 27 of his October 11, 2007  
22 Declaration, that "many memory chip manufacturers were already building some types of probe  
23 card resource sharing in house (San Disk, Samsung, Hynix), or hiring other companies  
24 (Formfactor, TouchDown Technologies, and TSE) to work with them." First, if I had believed  
25 that these companies were working on the same product, I would not have invested so much time  
26 and effort into developing the Picasso ASIC. Second, I did not have any knowledge of what  
27 Samsung, Hynix, Formfactor or TSE are doing in this area or even if they are doing anything in  
28 this area.

1           4.     There is a lot of cross-over in the tester business, and although it is my  
2 understanding that Verigy's main business is in selling tester machines, they also have interests in  
3 probe cards. [REDACTED]

4 [REDACTED]. I have personal  
5 knowledge of this fact because I am on the board of directors of Touchdown.

6           5.     I am friends with Alan Hart, Edmundo de la Puente and Gayn Erickson. I do  
7 occasionally run with Alan Hart and/or Edmundo de la Puente. However, I do not and would not  
8 discuss product roadmaps or technical research and development information relating to Verigy  
9 with them. I consider this information to be highly confidential and proprietary.

10          6.     In fact, when I worked at Agilent, it was my understanding and experience that  
11 documents and information were always treated as confidential unless it was explicitly  
12 communicated that it was permitted to publicly share the information or documents. I followed  
13 that general policy and it was my experience that my employees followed that general policy as  
14 well.

15          7.     In my experience, memory chip manufacturers are very guarded with information  
16 about testing their chips. Although some general chip information is publicly available on their  
17 websites or data sheets, the kind of detailed information necessary to make testers work with their  
18 chips is generally disclosed only pursuant to a non-disclosure agreement [REDACTED]

19 [REDACTED]  
20          8.     On August 6, 2006, I received an email from Mayder enclosing [REDACTED]. A  
21 true and correct copy of the email and attachment is attached hereto as Exhibit 1. In the email,  
22 sent from Mayder's silicontests.com email address, [REDACTED]  
23 [REDACTED] Ayashi was a new system being introduced by  
24 Advantest. Advantest is another company in the chip testing business. I had heard that Ayashi  
25 would significantly increase parallel testing at wafer sort and this would likely result in a smaller  
26 market for the [REDACTED] I therefore wanted to learn more about the system before making a  
27 financial investment. I never asked Mayder to send it to me so I could [REDACTED]  
28

1 [REDACTED] was not then and I am not now aware of Verigy's product  
2 roadmap.

3 9. Mayder initially named the product [REDACTED]" and we called it the [REDACTED]  
4 internally, but we also used several different names for the [REDACTED] in our external  
5 presentations to customers, including [REDACTED]

6 [REDACTED]  
7 [REDACTED] It was merely the name we used for  
8 external communications.

9 10. I have reviewed a data sheet from a version of the [REDACTED] I  
10 understand Mayder currently calls "Flash Enhancer." Attached hereto as Exhibit 2 is a true and  
11 correct copy of the Flash Enhancer data sheet I reviewed. This datasheet reflects that there have  
12 been some new features added to the ASIC. However, based on my experience, I believe that  
13 these changes are the types of modifications or refinements that customarily occur in response to  
14 supplier issues and/or customer requirements over the design cycle of any ASIC as it progresses  
15 from inception to first silicon. The key features, [REDACTED]

16 [REDACTED]  
17 [REDACTED] This "Flash Enhancer" datasheet appears to reflect an expected evolution of the same  
18 product Mayder and I worked on in June 2006.

19 11. In addition to the "Flash Enhancer" datasheet, I reviewed a number of documents  
20 relating to the [REDACTED] including (1) the June 12, 2006 RFQ and technical specification,  
21 attached to my previous declaration as Exhibit A; (2) Mayder's August 2006 draft patent  
22 disclosure, attached to my previous declaration as Exhibit F; (3) the [REDACTED]  
23 [REDACTED]  
24 [REDACTED] is attached hereto as Exhibit 3); and (4) the  
25 [REDACTED] sent to me on  
26 November 30, 2006 (a true and correct copy of [REDACTED] is attached hereto as Exhibit  
27 4). These documents show the status of the [REDACTED] certain points in time.  
28

1           12.    Based on my review of these documents, the only changes apparent to me that are  
2 not contained in the [REDACTED]

3 [REDACTED]  
4 [REDACTED]  
5 [REDACTED]  
6 [REDACTED]  
7 [REDACTED]  
8 [REDACTED] Attached hereto as Exhibit 5 is a true and correct copy of a chart I  
9 created showing the features of the [REDACTED] at these various points in time.

10           13.    Mayder's October 11, 2007 Declaration (specifically paragraphs 8 and 44)  
11 inaccurately describes the testing requirements for NOR flash vs. NAND flash. NOR and NAND  
12 are both flash memory and are often tested using the same testers and probe cards. In contrast,  
13 DRAM, SRAM and MRAM memory chips are very different from NOR and NAND memory  
14 chips, and are typically tested using completely different testers and probe cards than the NOR and  
15 NAND chips. In addition, the number of pins on a device is typically a function of the type of  
16 "interface" the device uses, and not strictly the type of flash memory. A serial interface uses  
17 fewer pins than a parallel interface. Both NOR and NAND devices can be made with either type  
18 of interface. For example, there are NOR devices in both parallel and serial interfaces. NAND  
19 devices can also have a variety of interfaces. There are serial NOR devices with only 8 pins and  
20 there are some that have over 64 pins. Therefore, Mayder's claims in paragraph 8 of his  
21 Declaration that to test NOR memory chips, the [REDACTED] would need to have "32 or 64 pins  
22 dedicated to addressing," and "four to eight times the number of channels to test the device" are  
23 simply not accurate.

24           14.    Furthermore, most of the differences between testing NOR and NAND memory  
25 chips are addressed in the tester software and not in hardware such as the [REDACTED]. In fact,  
26 when I was involved in developing the [REDACTED] we were designing the ASIC to work on  
27 either NOR or NAND. The only real difference was the number of signal vs. power switches, not  
28 the design of the ASIC or its topology.

1           15.     Mayder and I discussed development of an ASIC that would test both NAND and  
2     NOR from the very beginning. Attached hereto as Exhibit 6 is a copy of a July 24, 2006 draft  
3     presentation for potential customers for the [REDACTED] that Mayder created that discusses both  
4     NAND and NOR testing.

5           16.     In July and August of 2006, I was extremely busy with issues involving my own  
6     company, Attest Technologies. During these months, I did not devote much time or energy to  
7     Mayder and Silicon Test Solutions ("STS"). Mayder was very concerned with protecting the  
8     intellectual property we had been discussing. [REDACTED]

9     [REDACTED]  
10    [REDACTED] as soon as possible, and while I agreed that this was a good plan, I did not initiate  
11    the process —Mayder did.

12           17.     On September 1, 2006, Mayder and I received [REDACTED]  
13     [REDACTED]  
14     [REDACTED]  
15     [REDACTED] The September 1, 2006 [REDACTED]  
16     [REDACTED] and an initial per chip price of \$ [REDACTED] The NRE is a one  
17     time, up-front cost that manufacturers charge to cover the costs of researching, designing and  
18     testing a new product.

19           18.     On September 19, 2006, [REDACTED]  
20     [REDACTED] A true and correct copy of the September 19, 2006 email from [REDACTED]  
21     attached hereto as Exhibit 8.

22           19.     On November 20, 2006, Mayder sent me an email forwarding to me [REDACTED]  
23     November 19, 2006 revised proposal. A true and correct copy of Mayder's November 20, 2006  
24     email to me is attached hereto as Exhibit 9. The November 19, 2006 proposal shows a [REDACTED]  
25     [REDACTED]

26           20.     It is my understanding that as of at least September 8, 2006, Daniel Hanley, Esq. of  
27     San Jose represented Mayder and the STS Companies. Mr. Hanley was the attorney who formed  
28

1 the LLC for STS on September 8, 2006. Mayder informed me at that time that he was consulting  
2 Mr. Hanley regarding issues involved in incorporating STS.

3 21. On September 25, 2006, Mayder and I met with Thomas Schneck, Esq., to discuss

4 [REDACTED] Mayder told me that he had concerns about [REDACTED]  
5 [REDACTED]  
6 [REDACTED]

7 22. I decided I needed to consult my own attorney, and so I contacted Heather Flick,  
8 Esq., in early September 2006 to seek her advice regarding my potential investment and  
9 partnership with Mayder and to make sure that there weren't any legal issues I should be  
10 concerned about. However, I did not retain Ms. Flick until September 20, 2006.

11 23. Mayder and I did not meet with Ms. Flick on September 6, 2006 and in fact,  
12 Mayder never met with her. On September 6, 2006, [REDACTED]  
13 [REDACTED]. Attached hereto as Exhibit 10 is a true and correct copy  
14 of my Outlook calendar for June-September 2006 (with non-relevant, private meeting redacted).  
15 Exhibit 10 confirms my September 6, 2006 meeting with [REDACTED]

16 24. Mayder sent some information to Ms. Flick at my request, including a copy of  
17 someone else's Agreement Regarding Confidential Information and Proprietary Developments  
18 ("ARCIPD"). Mayder never sent his actual ARCIPD to me or to Ms. Flick.

19 25. On September 28, 2006, Mayder and I participated in a conference call with Ms.  
20 Flick so that she could advise me regarding my potential investment in STS. This was the first  
21 time (and to my knowledge, the only time) Mayder spoke with Ms. Flick regarding my potential  
22 investment in STS and the possible legal issues involved. Ms. Flick made it very clear during that  
23 call that she was representing me and not Mayder or STS. [REDACTED]  
24 [REDACTED]  
25 [REDACTED]  
26 [REDACTED]  
27 [REDACTED]  
28 [REDACTED]

1 [REDACTED]  
2 [REDACTED]  
3 [REDACTED]  
4 26. Mayder never informed Ms. Flick or me that Verigy or Agilent had ever had any  
5 projects related to the type of "resource sharing" for which the [REDACTED] designed or that  
6 Verigy had engaged in discussions [REDACTED]. In fact, in a  
7 September 20, 2006 email from Mayder to Ms. Flick and me, [REDACTED]

8 [REDACTED]  
9 [REDACTED]  
10 [REDACTED]  
11 [REDACTED]  
12 [REDACTED]  
13 [REDACTED] which I now know to be  
14 incorrect. Attached hereto as Exhibit 11 is a true and correct copy of Mayder's September 20,  
15 2006 email to Ms. Flick and me.

16 27. [REDACTED]  
17 [REDACTED]  
18 [REDACTED]  
19 [REDACTED]

20 I declare under penalty of perjury under the laws of the United States that the foregoing is  
21 true and correct.

22 Executed this \_\_\_\_ day of November, 2007 in Sunnyvale, California.  
23  
24

25 \_\_\_\_\_  
Robert Pochowski  
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4 26. Mayder never informed Ms. Flick or me that Verigy or Agilent had ever had any  
5 projects related to the type of "resource sharing" for which the Picasso ASIC was designed or that  
6 Verigy had engaged in discussions with Honeywell for a virtually identical ASIC. In fact, in a  
7 September 20, 2006 email from Mayder to Ms. Flick and me, Mayder informed us that Agilent

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13 , which I now know to be  
14 incorrect. Attached hereto as Exhibit 11 is a true and correct copy of Mayder's September 20,  
15 2006 email to Ms. Flick and me.

16 27.  
17  
18  
19

20 I declare under penalty of perjury under the laws of the United States that the foregoing is  
21 true and correct.

22 Executed this 15<sup>th</sup> day of November, 2007 in Sunnyvale, California.  
23

24   
25 Robert Pochowski  
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7  
DECLARATION OF ROBERT POCHOWSKI  
CASE NO. 07-04330 RMW (HRL)

**EXHIBIT 1**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER**  
**SEAL**

**EXHIBIT 2**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER  
SEAL**

**EXHIBIT 3**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER  
SEAL**

**EXHIBIT 4**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER  
SEAL**

**EXHIBIT 5**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER**  
**SEAL**

**EXHIBIT 6**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER  
SEAL**

**EXHIBIT 7**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER  
SEAL**

**EXHIBIT 8**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER  
SEAL**

**EXHIBIT 9**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER  
SEAL**

**EXHIBIT 10**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER**  
**SEAL**

**EXHIBIT 11**  
**TO POCHOWSKI DECLARATION**

**CONFIDENTIAL**

**EXHIBIT FILED UNDER**  
**SEAL**